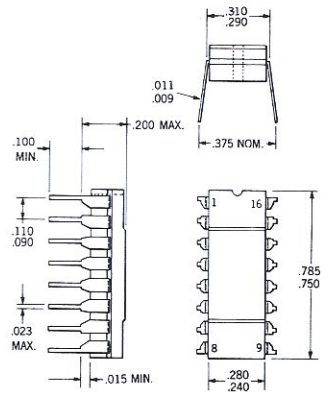
9301
MSI ONE-OF-TEN DECODER
A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9301 is a multipurpose decoder designed to accept four inputs and provide 10 mutually exclusive outputs. The circuit uses TTμL for high speed and high fan out capability, and is compatible with all members of the CCSL group of digital integrated circuits.

- **Multi-function capability**
- **Mutually exclusive outputs**
- **Guaranteed fanout of 10 TTμL loads over the full temperature range and supply voltage ranges**
- **High capacitive drive capability**
- **Demultiplexing capability**
- **Typical power dissipation of 145 mW**
- **The input/output characteristics provide easy interfacing with Fairchild DTμL, LPDTμL and TTμL families (CCSL).**
- **All ceramic "HERMETIC" 16-pin Dual In-Line* package**
- **Input clamp diodes limit high speed line termination effects**

PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

Fig. 1

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

LOGIC SYMBOL

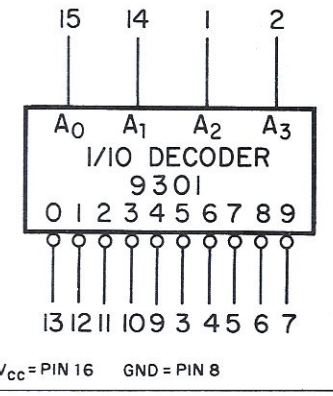


Fig. 2

ORDER INFORMATION

Specify U6B9301XXX for 16 pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

*Fairchild patent pending.

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MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3015048, 3025589, 3064167, 3108359, 3117260; OTHER PATENTS PENDING.

FUNCTIONAL DESCRIPTION

The 9301 Decoder accepts four active high BCD inputs and provides ten mutually exclusive active low outputs, as shown by Figure 2. The active low outputs facilitate memory addressing when inverting drivers are used between decoder and memory elements such as the 9033.

The logic design of the 9301 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant A_3 input produces a useful inhibit function when the 9301 is used as a 1 out of 8 decoder. This is illustrated in the 1 out of 32 decoder shown in Figure 9.

The Truth Table and Loading Rules for the 9301 are shown in Table I and Table II.

TABLE I — TRUTH TABLE

A_0	A_1	A_2	A_3	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Voltage Level
L = Low Voltage Level

TABLE II —

LOADING RULES (1 U.L. = TTμL Gate Input Load)

INPUTS	LOADING
A_0, A_1, A_2 & A_3	1 U.L.

OUTPUTS	FANOUT
0, 1, 2, 3, 4, 5, 6, 7, 8, & 9	10 U.L.

TABLE III —

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) (Part #U6B930151X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.10	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
t_{pd+} t_{pd-}	Turn Off Delay Input to Output Turn On Delay Input to Output				23 20	35 30			ns ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ See Fig. 8

TABLE IV —

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) (Part #U6B930159X)

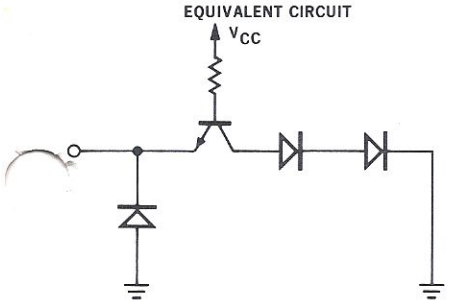
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$ $V_{CC} = 5.25\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
			−1.41		−0.9	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
t_{pd+}	Turn Off Delay Input to Output				23	35			ns	$V_{CC} = 5.0\ V$
t_{pd-}	Turn On Delay				20	30			ns	$C_L = 15\ pF$ See Fig. 8

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

Fig. 3

INPUTS

EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

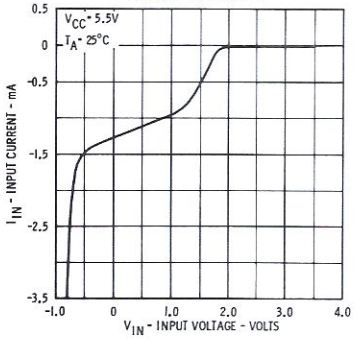
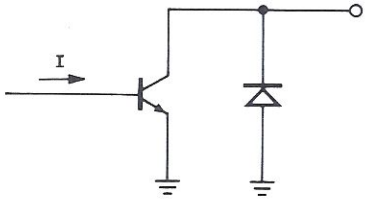


Fig. 4

OUTPUTS

EQUIVALENT CIRCUIT

OUTPUT LOW



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW

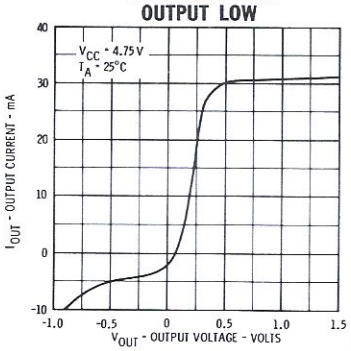
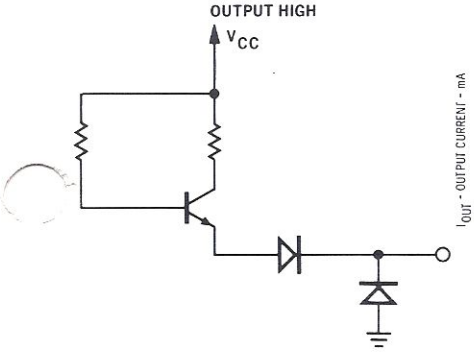
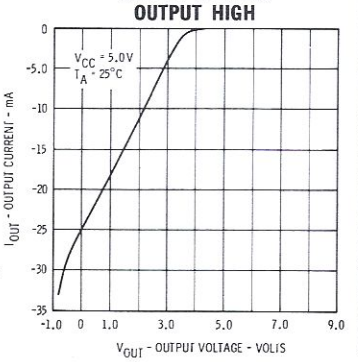


Fig. 5

OUTPUT HIGH



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH



SWITCHING PERFORMANCE

Fig. 6

TYPICAL TURN ON DELAY VERSUS TEMPERATURE

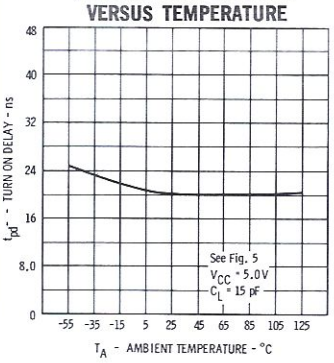
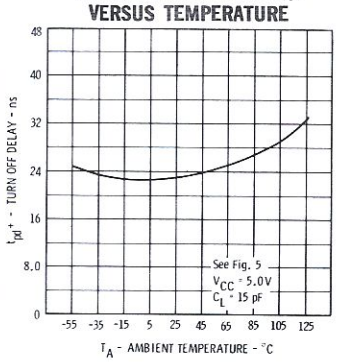
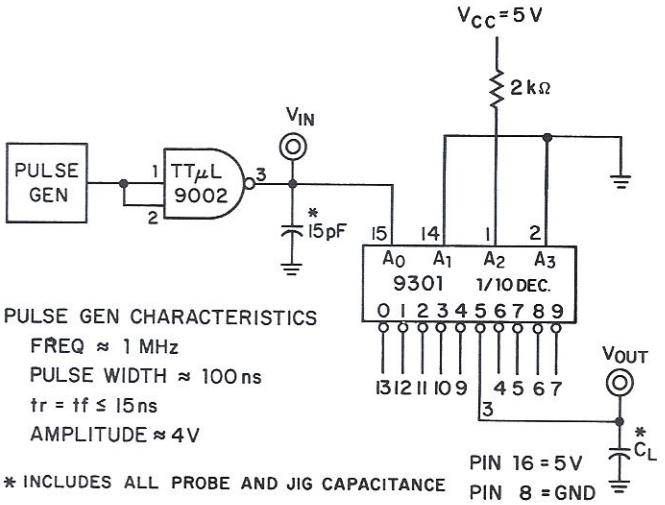


Fig. 7

TYPICAL TURN OFF DELAY VERSUS TEMPERATURE





PULSE GEN CHARACTERISTICS
- FREQ ≈ 1 MHz
- PULSE WIDTH ≈ 100 ns
- tr = tf ≤ 15 ns
- AMPLITUDE ≈ 4 V

* INCLUDES ALL PROBE AND JIG CAPACITANCE

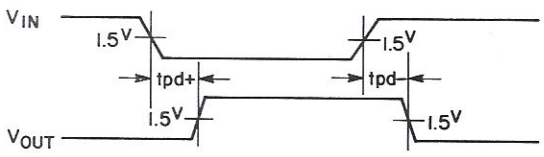


Fig. 8 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

APPLICATIONS — The 9301 decoder may be used for BCD to Decimal or 3 bit binary to octal conversion as well as many other applications. The general purpose nature of the 9301 is indicated by its use in the following applications.

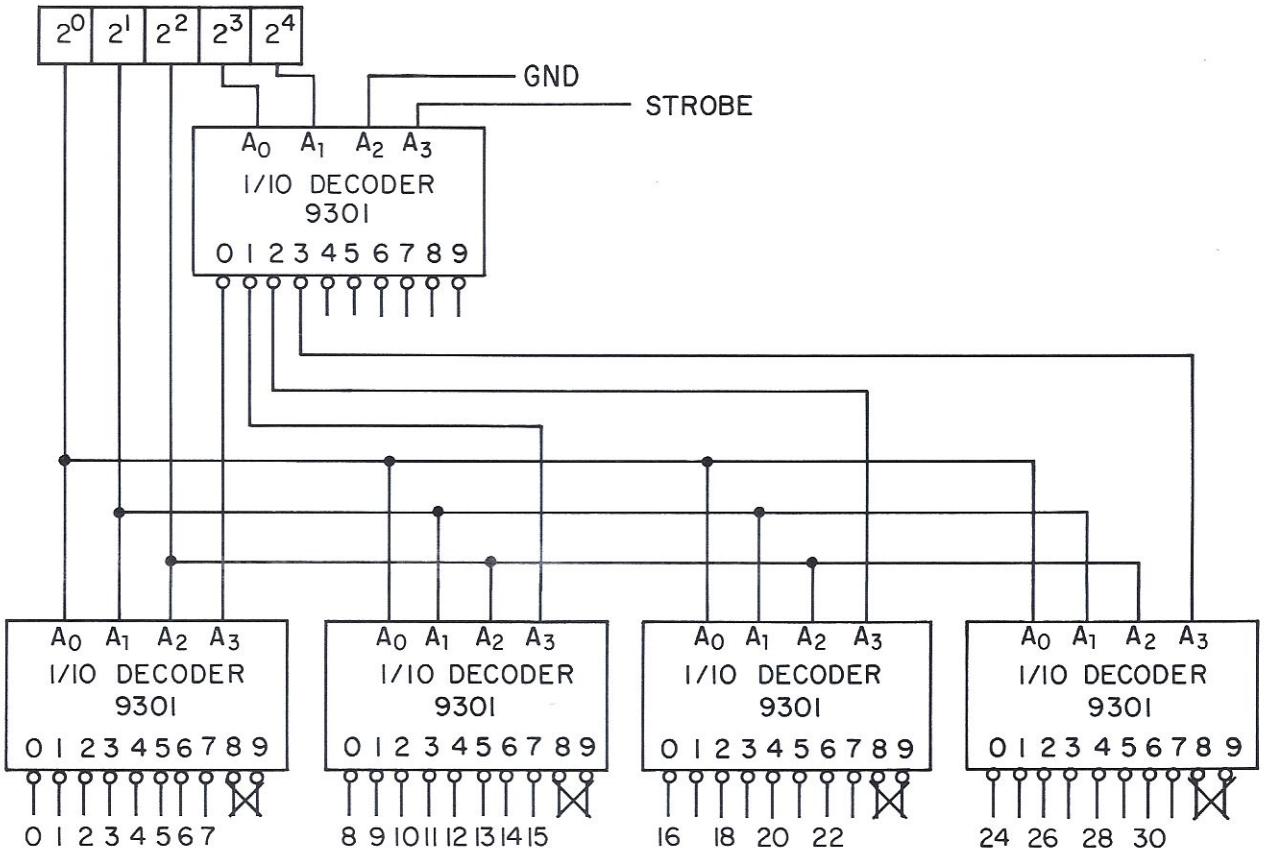
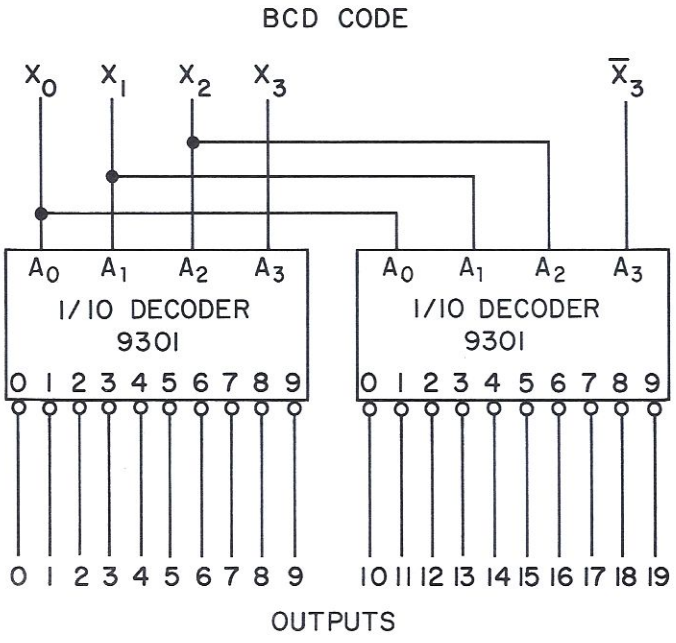


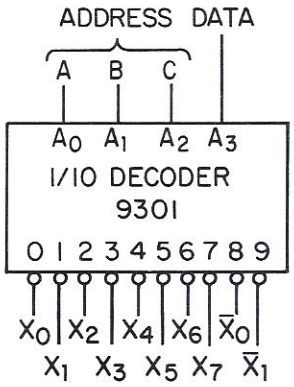
Fig. 9 — ONE-OUT-OF-THIRTY-TWO DECODING



DECIMAL DIGIT	OUTPUT SELECTION BCD CODE 8421	5421	EXCESS 3	4221
0	0, 18	0, 18	3	0, 18
1	1, 19	1, 19	4	1, 19
2	2	2	5	2
3	3	3	6	3
4	4	4	7	6
5	5	8, 10	8, 10	9, 11
6	6	9, 11	9, 11	14
7	7	12	12	15
8	8, 10	13	13	16
9	9, 11	14	14	17

Decode any BCD code using two 9301 elements. Any 4 bit BCD code may be decoded by selecting outputs as shown in the table.

Fig. 10 — DECODE ANY BCD CODE

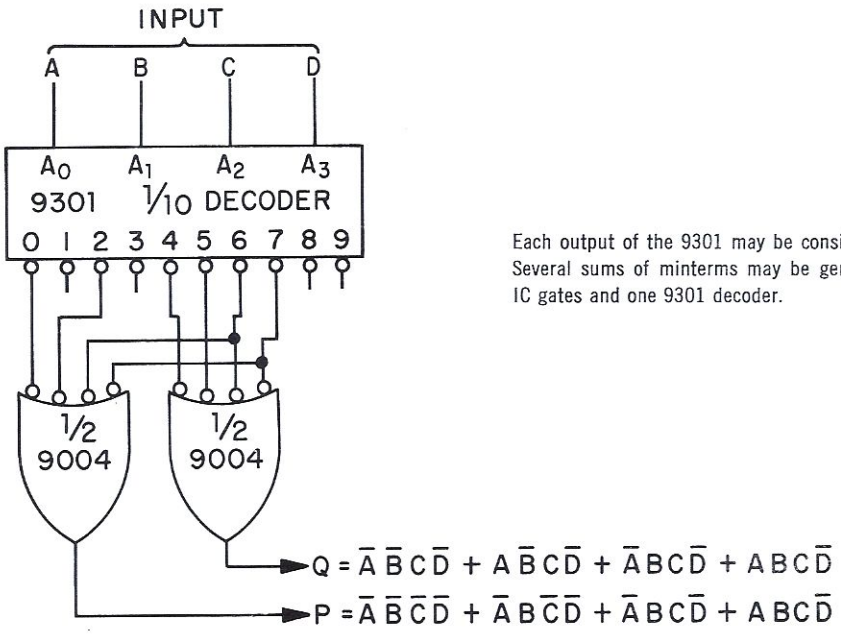


ADDRESS			OUTPUT LINE
A	B	C	
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

Data may be routed from a source to any of 8 outputs by addressing that output. All non-addressed outputs remain high.

Complements of outputs 0 and 1 are available at outputs 8 and 9 respectively.

Fig. 11— DIGITAL DEMULTIPLEXER



Each output of the 9301 may be considered a minterm of the input code. Several sums of minterms may be generated economically using discrete IC gates and one 9301 decoder.

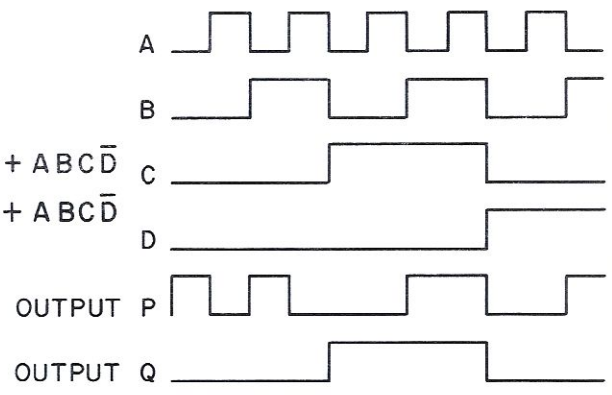


Fig. 12— MINTERM GENERATOR

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